

# An LDMOS VHF Class-E Power Amplifier Using a High- $Q$ Novel Variable Inductor

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**Abstract**— In this paper, an lateral diffused metal–oxide–semiconductor-based very high-frequency class-E power amplifier has been investigated theoretically and experimentally. Simulations were verified by amplifier measurements and a record-high class-E output power was obtained at 144 MHz, which is in excellent agreement with simulations. The key of the results is the use of efficient device models, simulation tools, and the invention of a novel high- $Q$  inductor for the output series resonance network. The latter allows for low losses in the output network and, simultaneously, a wide tuning range for maximum output power or maximum efficiency optimization.

**Index Terms**—High efficiency, power amplifier.

## I. INTRODUCTION

THE class-E amplifier is an attractive solution to obtain a high output power with a high efficiency; the principle of the circuit was first described by Ewing [1] in 1964. Ewing demonstrated an amplifier with 20-W output power with 94% efficiency at 500 kHz.

Eleven years later, Sokal and Sokal [2] showed an amplifier working in the low megahertz range with 26-W output power and a drain efficiency of 96%. Closed-form equations have been developed by many authors to aid the design of the class E-amplifier [3]. Due to the evolution of advanced MOS transistor technologies like lateral diffused metal–oxide–semiconductor (LDMOS), and the increasing demand of high-efficiency amplifiers for mobile communication, the class-E concept is again receiving attention, and output powers of up to 400 W have been obtained in the high-frequency band [4]. In the VHF range and higher, some experimental results have been obtained, but the output power has thus far been limited [5], [6]. In this paper, a novel concept of the output network and the usage of the newly developed Silicon LDMOS device made it possible to achieve a record-high output power of 54 W with a comparatively high efficiency of 70% at a frequency of 144 MHz. We believe that the results can be scaled up both in power and frequency.

## II. THE CLASS-E AMPLIFIER

The switched-mode class-E amplifier is ideally based on the characteristic topology, according to Fig. 1, where a switch

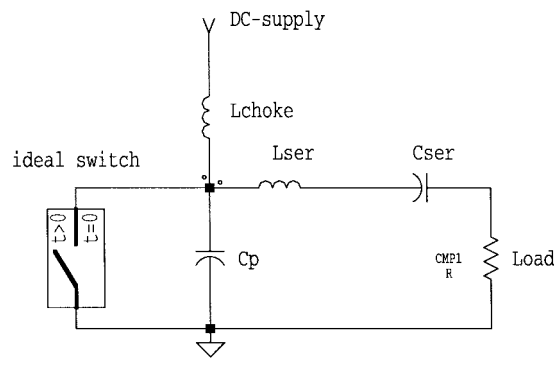


Fig. 1. Ideal class-E amplifier circuit.

is charging a choke with magnetic energy during the “on” time of the switch, while during the “off” time, the energy is released partly to the parallel capacitor  $C_p$  and partly to the output network, which consists of a load in series with a series resonance circuit. In our work, the switch is realized by an LDMOS transistor driven by a voltage applied at the gate. At frequencies in the VHF band and higher, neither the switch nor the passive components can be regarded as ideal, and the analytical equations described by different authors cannot be used anymore for successful optimization of the circuit. However, the recent improvements in the modeling of active devices and simulation tools have made it possible to design such amplifiers with sufficiently good accuracy by computer simulation. The LDMOS transistor used in this study is an MRF 183 from Motorola, which is able to deliver an output power of 45 W with 33% drain efficiency at 900 MHz. A nonlinear model based on the Root model is available on Motorola’s website and can be easily downloaded to the simulator.

In order to obtain a practical class-E amplifier topology some modifications to Fig. 1 had to be made. The goal was to obtain the same power from the transistor compared to when it is working in class AB and to investigate the possibility of achieving a high efficiency simultaneously. The capacitor  $C_p$  is partly absorbed by the transistor through its output capacitance, which for the particular device is 38 pF. The input impedance according to the datasheet is quite low,  $1.1 + j0.93 \Omega$  (at 930 MHz) so a matching network consisting of a ferrite transformer and a series inductor was used at the input. A turn ratio of four was used in the simulations. In order to increase the output power to the load, the 50- $\Omega$  load impedance was transformed to 1.5  $\Omega$  by a parallel capacitance and a series inductance. This series inductance is absorbed

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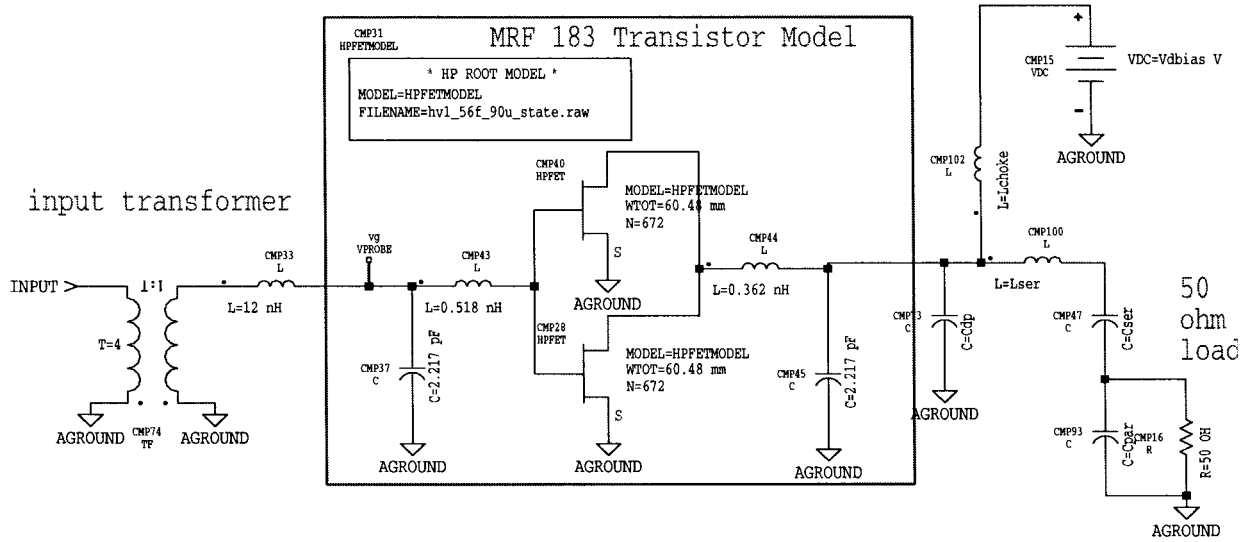


Fig. 2. Class-E amplifier circuit.

TABLE I  
COMPONENT VALUES OF THE OPTIMIZED DESIGN

Cdp (pF)	Lchoke (nH)	Lser (nH)	Cscr (pF)	Cpar (pF)
55	100	24	120	100

in the series resonance circuit. The  $Q$ -value of the resonance circuit was chosen to be low, of the order of five, in order to have reasonable bandwidth and low sensitivity of the circuit performance to the series resonator values.

### III. SIMULATIONS

The device model was inserted in the simulator and the circuit topology in Fig. 2 was used for the simulation and optimization of the circuit. The impedance transforming network at the output was determined by a linear simulation, while the choke  $L_{choke}$  and the capacitor  $C_{dp}$  were optimized for highest efficiency at maximum output power.  $L_{choke}$  was chosen to have the smallest possible value without sacrificing the efficiency. Component values of the optimized design are listed in Table I.

The operation of a class-E amplifier is determined by the series resonance network, i.e., the output power and the efficiency is critically dependent on the tuning of this network. The output power, efficiency, and different waveforms were, therefore, investigated as a function of the inductance of the series resonance. Fig. 3 shows the output power and Fig. 4 the drain and power-added efficiency when this inductor is swept from 10 to 30 nH. Point *b*) refers to high output power while points *a*) and *c*) are points tuned out from the resonance. It is clear from the figures that the highest efficiency is obtained at a higher value of  $L_s$  than the value obtained at maximum power, i.e., the resonance circuit should be tuned somewhat lower in frequency compared to the input frequency in order to obtain high efficiency. The predicted maximum drain efficiency is 92% at an output power of 20 W. At the maximum power point, i.e., 60 W, the drain efficiency is 70%. From this

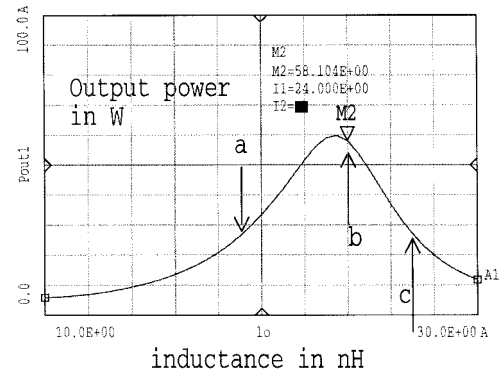


Fig. 3. Output power (in watts) versus series inductance.

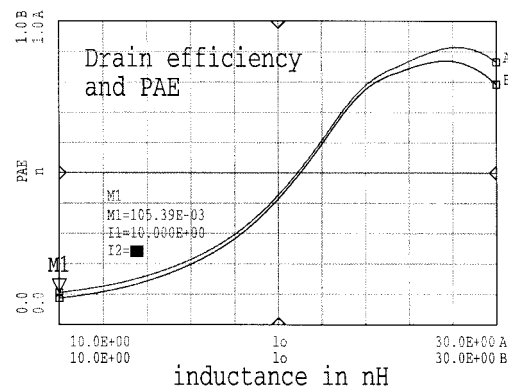


Fig. 4. Drain efficiency and power-added efficiency versus series inductance.

simulation, it is clear that the output power can be readily tuned by the series resonance inductor. The drain voltage, the sum of the currents through the device and  $C_{pd}$ , and the gate voltage at points *a*)–*c*) is shown in Fig. 5. The power is approximately the same for the *a*) and *c*) cases, but the efficiency is optimum for *c*). Note the high choke-current in case *a*) compared to case *c*). Also note the absence of ringing

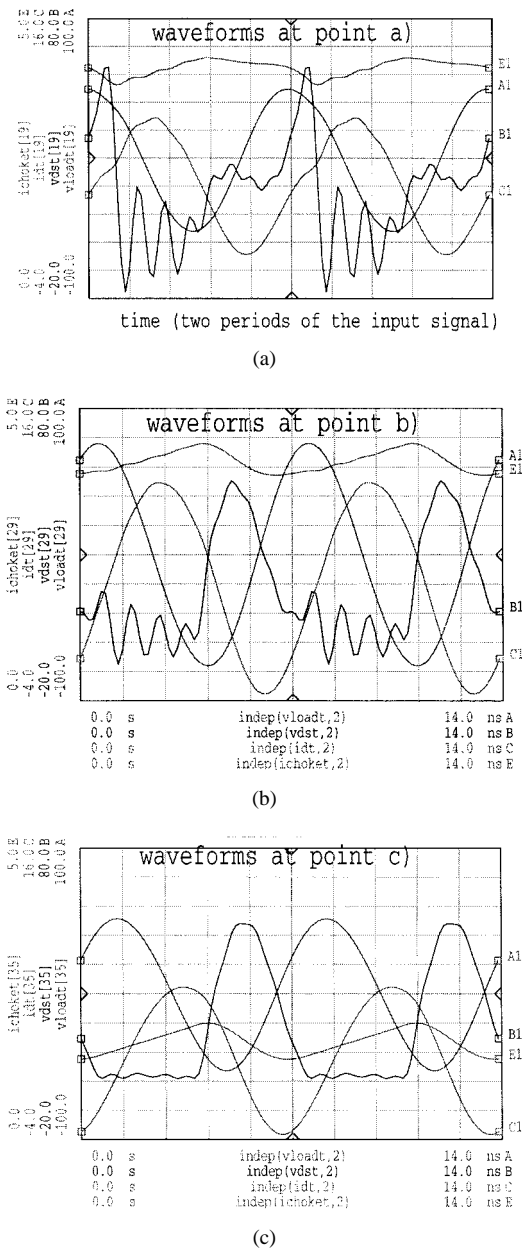


Fig. 5. (a) Waveforms: choke current ( $i_{choket}$ ), drain current ( $i_{dt}$ ), drain voltage ( $v_{dst}$ ), and load voltage ( $v_{loadt}$ ) for point *a*) in Fig. 3. (b) Waveforms for point *b*) in Fig. 3. (c) Waveforms for point *c*) in Fig. 3.

in the drain voltage waveform when the device is in its on state, when  $L_s$  is tuned optimally [case *c*]]. At maximum power, the peak current through the transistor and  $C_{pd}$  is 11 A with a mean value of about 4 A.

#### IV. DESIGN OF THE AMPLIFIER

When all component values were optimized, passive components were selected from the basis of  $S$ -parameter characterization.  $L_d$  was fabricated by using a tinned wire with a diameter of 0.5 mm, and the input transformer was made by using a binocular-type nickel–zinc ferrite of type Fair-rite 28 43 002 402. For all capacitors, except the  $V_{dd}$  decoupling capacitors, ATC-100 capacitors were used. All components were tested on an HP 8510 vector network analyzer (VNA)

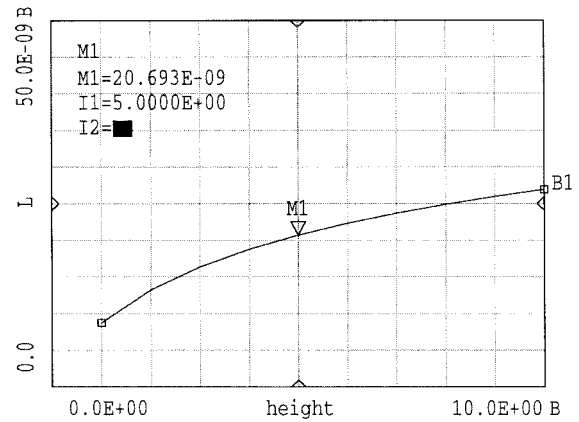


Fig. 6. Inductance of 50-mm-long ribbon with a 4 mm  $\times$  1 mm cross section versus distance from ground in millimeters.

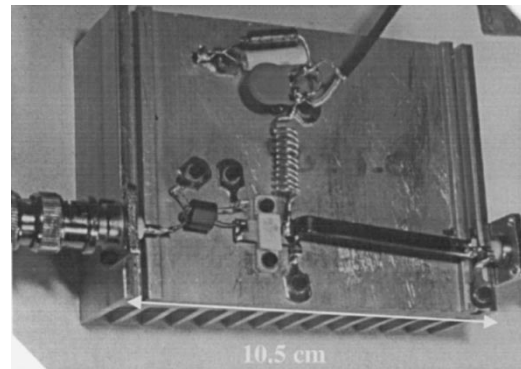


Fig. 7. Photo of the amplifier.

for verification. Since simulations predicted that the circuits are critically dependent of the output series resonance circuit, special care was taken in the design of this part. A novel inductor was invented, using a copper ribbon 5 mm above the ground plane. By inserting a wedge-shaped aluminum tuning plate between the ribbon and ground plane, the inductance can be tuned by at least a factor of two. The  $Q$  value of the inductor, as measured by the VNA, is more than 500 at 144 MHz, somewhat dependent on the distance to the ground plane. Fig. 6 shows the simulation of the inductance versus distance from the ground plane for a 5-cm-long ribbon with a cross section of 4 mm  $\times$  1 mm. This result was also experimentally verified in a special fixture. The transistor was mounted on a heatsink and all components were connected by soldering (see Fig. 7). After assembling the circuit, the amplifier was connected to the bias supply and measurement equipment and the amplifier worked immediately.

#### V. EXPERIMENTAL RESULTS

The frequency of the generator was set to 144 MHz and the input and output power was measured with a Bird 4421 power meter, which has an accuracy of  $\pm 3\%$ . The output versus input power was first measured and the output inductance was tuned for maximum power. The data from this measurement is plotted in Fig. 8. The drain supply voltage was 20 V. From

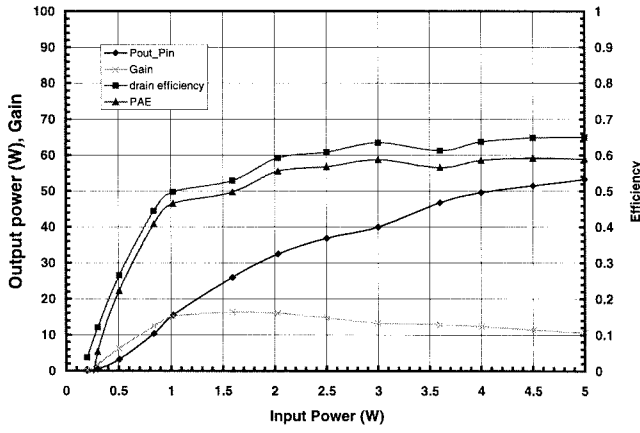


Fig. 8. Output power, gain, drain efficiency, and power-added efficiency as a function of input power at 144 MHz.

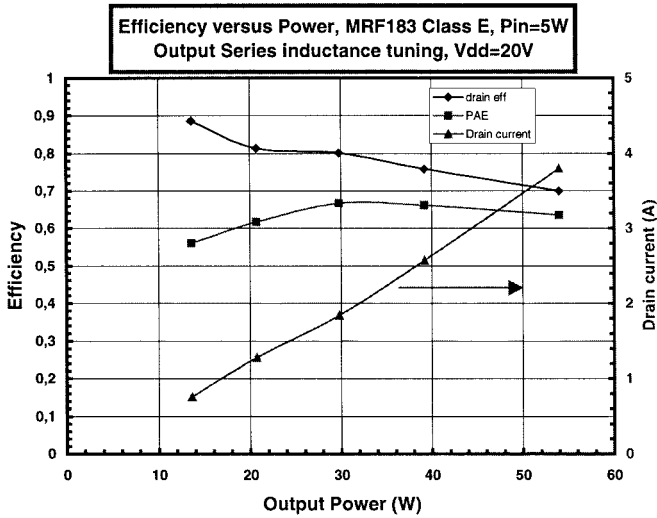


Fig. 9. Efficiency and drain current versus output power. This plot is made by varying the series inductance.

the figure, we can conclude that an input power of 5 W was needed in order to achieve saturated operation, i.e., a state where the output power is not too dependent on the input power. The drain efficiency and power-added efficiency are relatively constant from 3 to 5 W.

In the next measurement, the input power was kept constant to 5 W, while the output inductance was tuned manually by changing the position of the tuning plate. The result of this measurement is plotted in Fig. 9, which shows the output power, drain supply current, drain efficiency, and power-added efficiency *versus the tuning of the series inductance*, i.e., the amplifier is tuned between the high-efficiency point toward the high power point, as was described in the theory (point *b*) to point *c*) in Fig. 4). As can be seen from the figure, the power and efficiency behavior is similar to the simulations with a maximum power of 54 W and an associated drain efficiency of 70%. The experimental efficiency is increasing when  $L_s$  is increased from the maximum power point in accordance with the theory, at 14-W output power, the drain efficiency is 88%. The power-added efficiency is decreasing at low output power levels since the output power is decreased, while the

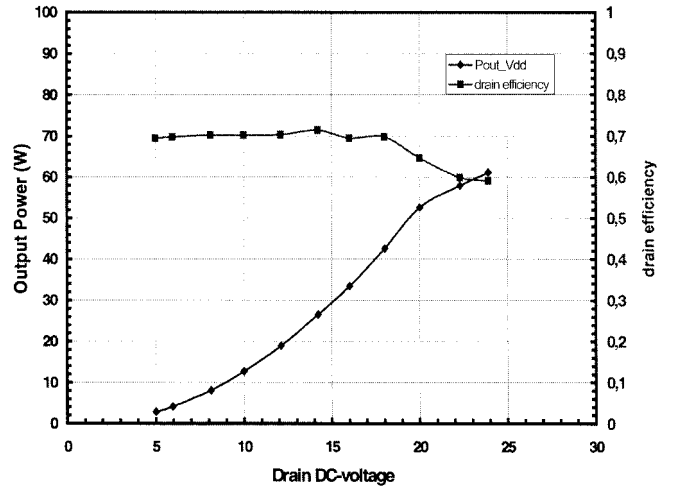


Fig. 10. Output power and drain efficiency as a function of the drain supply voltage.

input power is constant. Decreasing the input power could possibly increase the power-added efficiency, but this was not investigated in this study.

One interesting feature with the class-E amplifier is the variation of the output power versus the drain supply voltage. The peak drain voltage is of the order three times the drain supply voltage, as can be seen from the waveform simulations, up to a point when the drain-breakdown voltage is reached. In Fig. 10, the output power and drain efficiency is plotted as a function of the drain supply voltage. The drain efficiency is constantly between 5–18 V. Supported by the simulations, we believe the decrease of the efficiency above  $V_{dd} = 18$  V is due to breakdown in the transistor. The power versus drain supply voltage is clearly quadratic up to a point when the drain efficiency start to drop. The output spectrum was also monitored by an HP 8563 Spectrum analyzer. The second harmonic dominated and was typically 38 dB below the carrier.

## VI. SUMMARY

A class-E amplifier based on LDMOS transistors working at VHF was demonstrated by simulations and experiments. A record-high power was obtained in class E at this frequency, i.e., 62 W, from a single device with 121-mm gatewidth. At a lower power, i.e., 14 W, the drain efficiency was as high as 88%. The key of this result is proper tuning of the series resonator network, computer simulations with good models, and the use of a novel inductor design. The drain efficiency was experimentally found to be independent on the supply voltage up to the breakdown voltage of the transistor.

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**Herbert Zirath** (S'84–M'86), for photograph and biography, see this issue, p. 2357.